REMARKS

This application is a continuation application based on U.S. Application Serial No. 09/737,715 filed December 15, 2000. Support for new claims 4-51 may be found in the specification, for example, as follows:

- claims 4, 28 and 47 at page 1, line 15 through page 2, line 2 and page 35, line 25 through page 36, line 17;
- claims 5-27 and 48 at page 27, lines 4-16 and page 33, line 18 through page 34, line 19;
- claims 29-31 at page 16, line 20 through page 18 line 12;
- claim 32 at page 12, lines 11-17;
- claims 33-34 at page 18, lines 4-28;
- claims 35-46 at page 1, line 15 through page 2, line 2, page 19, line 1 through page 23 line 23 and page 35, line 25 through page 36, line 17;
- claim 49 at page 16, line 2 through page 17, line 6; and
- claims 50-51 at page 16 line 2 through page 18, line 28.

Favorable consideration and early allowance of all pending claims is requested.

* Applicant has enclosed a check in the amount of $1,412.00 to cover the fees to file this application. The Examiner is authorized to charge any underpayment or to credit any

overpayment of the above-referenced fees to Deposit Account No. 19-1345.

Respectfully submitted,

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*Enclosures

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

The title has been amended as follows:

SILICON ON INSULATOR STRUCTURE **[FROM]** **HAVING A** LOW DEFECT DENSITY **[SINGLE CRYSTAL SILICON]** **HANDLE WAFER AND PROCESS FOR THE PREPARATION THEREOF**.

IN THE SPECIFICATION:

The paragraph beginning at page 1, line 3 has been amended as follows:

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority from U.S. provisional application Serial No. 60/098,902, filed on September 2, 1998 **and U.S. application Serial Number 09/387,288 filed on August 8, 1999**.

IN THE ABSTRACT:

The text of the abstract beginning on page 63, line 1 has been amended as follows:

The present invention relates to a **process for the preparation of a** silicon on insulator **[("SOI") structure having a low defect density device layer and, optionally, a handle** wafer **having improved gettering capabilities]**. The **process includes implanting oxygen into a single crystal silicon wafer** **[**device

layer comprises a central axis, a circumferential edge, a radius extending from the central axis to the circumferential edge, and a first axially symmetric region] which is substantially free of agglomerated **[intrinsic point]** **vacancy-type** defects. **The present invention further relates to a process for the preparation of a silicon on insulator wafer wherein oxygen is implanted into a single crystal silicon wafer having an axially symmetric region in which there is a predominant intrinsic point defect which is substantially free of agglomerated intrinsic point defects.** Additionally, the present invention **relates** **[is directed]** to a **silicon on insulator ("SOI")** structure **in** which **the device layer and the [has a Czochralski single crystal silicon]** handle wafer which is capable of forming an ideal, non-uniform depth distribution of oxygen precipitates upon being subjected to the heat treatment cycles of essentially any arbitrary electronic device manufacturing process.

IN THE CLAIMS:

Claims 1 through 3 have been canceled.

New Claims 4 through 59 have been added.